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PATENT

Case Docket No. IMEC92.001DV1
Date: September 3, 2004

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s)	:	Brockmeyer, et al.
Appl. No.	:	10/766,159
Filed	:	Janaury 27, 2004
For	:	OPTIMIZED DATA TRANSFER AND STORAGE ARCHITECTURE FOR MPEG-4 MOTION ESTIMATION ON MULTI-MEDIA PROCESSORS
Examiner	:	Jose L. Couso
Group Art Unit	:	2621

I hereby certify that this correspondence and all marked attachments are being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on

September 3, 2004
(Date)

Eric M. Nelson, Reg. No. 43,829

TRANSMITTAL LETTER

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Enclosed for filing in the above-identified application are:

(X) An Information Disclosure Statement.

(X) A PTO Form 1449 with twenty-eight (28) references.

(X) The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment, to Account No. 11-1410.

(X) Return prepaid postcard.

Eric M. Nelson
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Attorney of Record
Customer No. 20,995
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INFORMATION DISCLOSURE STATEMENT

Applicant	:	Brockmeyer, et al.
App. No.	:	10/766,159
Filed	:	January 27, 2004
For	:	OPTIMIZED DATA TRANSFER AND STORAGE ARCHITECTURE FOR MPEG-4 MOTION ESTIMATION ON MULTI-MEDIA PROCESSORS
Examiner	:	Couso, Jose L.
Group Art Unit	:	2621

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Enclosed is form PTO-1449 listing 28 references that are also enclosed.

This Information Disclosure Statement is being filed before the receipt of a first Office Action on the merits, and presumably no fee is required in accordance with 37 C.F.R. § 1.97(b)(3). If a first Office Action on the merits was mailed before the mailing date of this Statement, the Commissioner is authorized to charge the fee set forth in 37 C.F.R. § 1.17(p) to Deposit Account No. 11-1410.

Respectfully submitted,

KNOBBE, MARTENS, OLSON & BEAR, LLP

Dated: 9/3/2004

By: _____

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FORM PTO-1449 U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DOCKET NO. IMEC92.001DV1	APPLICATION NO. 10/766,159
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (USE SEVERAL SHEETS IF NECESSARY)	APPLICANT Brockmeyer, et al.	
	FILING DATE January 27, 2004	GROUP Unknown

U.S. PATENT DOCUMENTS							
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE (IF APPROPRIATE)
	1.	5,978,509	11/02/99	Nachtergaele et al.			

EXAMINER INITIAL		OTHER DOCUMENTS (INCLUDING AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.)
	2	Agarwal, R. et al., Coding of moving pictures and audio, N1693 "International organization for standardization, ISO/IEC/JTC1/SC29WG11," April 1997.
	3	Amarasinghe, S. et al., "The SUIF compiler for scalable parallel machines," in *Proc. of the 7th SIAM Conf. on Parallel Proc. for Scientific Computing*, 1995.
	4	Bacon, D.F. et al., "Compiler transformations for high-performance computing," Computer Science Division, University of California, Berkeley, California, 1994.
	5	Brodersen, R.W., "The Network Computer and its Future," *Proc. IEEE Int. Solid-State Circ. Conf.*, San Francisco CA, pp.32-36, Feb. 1997.
	6	Catthoor, F. "Energy-delay efficient data storage and transfer architectures: circuit technology versus design methodology solutions," *Proceedings of DATE'98*, Feb.23-25 1998.
	7	Chandrakasan, A. et al., "Data driven signal processing: an approach for energy efficient computing," *Proc. IEEE Intnl. Symp. on Low Power Design, Monterey CA, pp.347-352, Aug. 1996.*
	8	Chatterjee, P. (President Personal Productivity Products, Texas Instruments), "Gigachips: deliver affordable digital multi-media for work and play via broadband network and set-top box," Plenary paper in *Proc. IEEE Int. Solid-State Circ. Conf.*, San Francisco CA, pp.26-30, Feb. 1995.
	9	Danckaert, K. et al., "System level memory optimization for hardware-software co-design," *Proc. IEEE Intnl. Workshop on Hardware/Software Co-design, Braunschweig. Germany, pp.55-59, March 1997.*
	10	De Greef, E. et al., "Memory organization for video algorithms on programmable signal processors," *Proc. IEEE Int. Conf. on Computer Design, Austin TX, pp.552-557, Oct. 1995.*
	11	Evans, R.J. et al., "Energy consumption modeling and optimization for SRAMs," *IEEE journal of solid state circuits*, vol 30, no 5, May 1995.
	12	Gannon, D., "Strategies for cache and local memory management by global program transformation," Journal of parallel and distributed computing 5, Academic press, pp.587-616, 1988.
	13	Itoh, K. et al., "Trends in low-power RAM circuit technologies," special issue on "Low power design" of the *Proceedings of the IEEE*, Vol. 83, No. 4, pp.524-543, April 1995.
	14	Kolson, D. et al., "Minimization of memory traffic in high-level synthesis," *Proc. 31st ACM/IEEE Design Automation Conf.*, San Diego CA, pp.149-154, June 1994.
	15	Lippens, P. et al., Allocation of multiport memories for hierarchical data streams," *Proc. IEEE Int. Conf. Comp. Aided Design*, Santa Clara CA, Nov. 1993.
	16	Meng, T.H. et al., "Portable video-on-demand in wireless communication," special issue on "Low power electronics" of the *Proceedings of the IEEE*, Vol.83, No.4, pp.659-680, April 1995.
	17	Moolenaar, D. et al., "System-level power exploration for MPEG-2 decoder on embedded cores : a systematic approach," *Proc. IEEE Wsh. on Signal Processing Systems (SIPS)*, Leicester, UK, Nov. 1997.
	18	Nachtergaele, L. et al., "Low power data transfer and storage exploration for H.263 video decoder system," accepted for special issue on *Very low-bit rate video coding* (eds. Argy Krikelis et al.) of *IEEE Journal on Selected Areas in Communications*, Vol.16, No.2, Feb. 1998.

EXAMINER	DATE CONSIDERED

*EXAMINER: INITIAL IF CITATION CONSIDERED, WHETHER OR NOT CITATION IS IN CONFORMANCE WITH MPEP 609; DRAW LINE THROUGH CITATION IF NOT IN CONFORMANCE AND NOT CONSIDERED, INCLUDE COPY OF THIS FORM WITH NEXT COMMUNICATION TO APPLICANT.

FORM PTO-1449 U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DOCKET NO. IMEC92.001DV1	APPLICATION NO. 10/766,159
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(USE SEVERAL SHEETS IF NECESSARY)	FILING DATE January 27, 2004	GROUP Unknown

EXAMINER INITIAL		OTHER DOCUMENTS (INCLUDING AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.)
	19	Nachtergaele, L. et al., "Optimisation of memory organisation and hierarchy for decreased size and power in video and image processing systems," *Proc. Intnl. Workshop on Memory Technology, Design and Testing*, San Jose CA, pp.82-87, Aug. 1995.
	20	Nachtergaele, L. et al., "System-level power optimization of video codecs on embedded cores : a systematic approach," accepted for special issue on *Future directions in the design and implementation of DSP systems* (eds. Wayne Burleson et al.) of *Journal of VLSI Signal Processing*, No., Kluwer, Boston, pp., Feb. 1998.
	21	Rabaey, J., "System-level power estimation and optimization - challenges and perspectives," *Proc. IEEE Intnl. Symp. on Low Power Design*, Monterey CA, pp.158-160, Aug. 1997.
	22	Seki, T. et al., "A 6-ns 1-Mb CMOS SRAM with Latched Sense Amplifier," IEEE J. of Solid-state Circuits, Vol.SC-28, No.4, pp.478-488, Apr. 1993.
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	24	Slock, P. et al., "Fast and extensive system-level memory exploration for ATM applications," *Proc. 10th ACM/IEEE Intnl. Symp. on System-Level Synthesis*, Antwerp, Belgium, pp.74-81, Sep. 1997.
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	28	Wolf, M. et al., "A loop transformation theory and an algorithm to maximize parallelism," *IEEE Trans. on Parallel and Distributed Systems*, Vol.2, No.4, pp.452-471, Oct. 1991.

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